Rajshekar K

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Personal Profile

I am currently an Assistant Professor in the Dept. of Computer Science and Engineering, IIT Dharwad. I have completed my PhD from IIT Delhi, and served as a Senior Research Fellow in the same department. My areas of interest include Computer Architecture, Trusted Systems, and Modelling and Simulation.

Employment

January 2018 - present	Assistant Professor, Dept. of Computer Science and Engineering, Indian Institute of Technology Dharwad, India
January 2017 - December 2017	Senior Research Fellow, Dept. of Computer Science and Engineering Indian Institute of Technology Delhi, India

Education

July 2012 - December 2016	Ph.D. in Computer Science and Engineering Indian Institute of Technology Delhi, India Thesis: Employing Redundancy based Techniques to Provide Reliability, Security and Accountability in Modern Processors

Publications

Journals

J1. A Formal Approach to Accountability in Heterogeneous Systems-on-Chip by Rajshekar Kalayappan, Smruti R. Sarangi, IEEE Transactions on Dependable and Secure Computing (TDSC). Volume 18 Issue 6, 2021.

J2. A Survey of Cache Simulators by Hadi Brais, Rajshekar Kalayappan, Preeti Ranjan Panda, ACM Computing Surveys (CSUR). Volume 53 Issue 1, 2020.

J3. ChunkedTejas: A Chunking-based Approach to Parallelizing a Trace-Driven Architectural Simulator by Rajshekar Kalayappan, Avantika Chhabra, Smruti R. Sarangi, ACM Transactions on Modeling and Computer Simulation (TOMACS). Volume 30 Issue 3, 2020.
Presented at ACM SIGSIM Principles of Advanced Discrete Simulations (PADS), 2022.

J4. Providing Accountability in Heterogeneous Systems-on-Chip by Rajshekar Kalayappan, Smruti R. Sarangi, ACM Transactions on Embedded Computing Systems (TECS). Volume 17 Issue 5, 2018.

J5. ParTejas : A Parallel Simulator for Multicore Processors by Geetika Malhotra, Rajshekar Kalayappan, Seep Goel, Pooja Aggarwal, Abhishek Sagar, Smruti R. Sarangi, ACM Transactions on Modeling and Computer Simulation (TOMACS). Volume 27, Issue 3, September 2017.

J6. FluidCheck: A Redundant Threading-Based Approach for Reliable Execution in Many-core Processors by Rajshekar Kalayappan, Smruti R. Sarangi, ACM Transactions on Architecture and Code Optimization (TACO). Volume 12 Issue 4, January 2016. Presented at European Network on High Performance and Embedded Architecture and Compilation Conference (HiPEAC'16), Prague, Czech Republic, 2016.

J7. Surveillance using non-stealthy sensors: A new intruder model by Amitabha Bagchi, Rajshekar Kalayappan, Surabhi Sankhla, Wiley Security and Communication Networks. Volume 7, Issue 11, November 2014.

J8. A survey of checker architectures by Rajshekar Kalayappan, Smruti R. Sarangi, ACM Computing Surveys (CSUR). Volume 45, Issue 4, August 2013.

Conferences

C1. CASH: Criticality-Aware Split Hybrid L1 Data Cache by Shruthi Karunakar, Meenakshi Atkade, Akash Poptani, Rajshekar Kalayappan, Sandeep Chandran, 34th ACM Great Lakes Symposium on VLSI (GLSVLSI'24), Tampa Bay Area, FL, USA, 2024.

C2. On Decomposing Complex Test Cases for Efficient Post-silicon Validation by Harshitha C, Sundarapalli Harikrishna, Peddakotla Rohith, Sandeep Chandran, Rajshekar Kalayappan, Asia and South Pacific Design Automation Conference (ASP-DAC'24), Incheon, South Korea, 2024. [Nominated for the best paper award]

C3. Enhancing the Dependability of Electronic Control Systems through Reprogrammable Runtime Verification Monitors by Amruta Benny, Sandeep Chandran, Rajshekar Kalayappan, Frontiers of Aerospace Systems and Technologies (FAST) 2023.

C4. SANNA: Secure Acceleration of Neural Network Applications by Akash Poptani, Abhishek Mittal, Rishit Saiya, Rajshekar Kalayappan, Sandeep Chandran, International Conference on VLSI Design and Embedded Systems (VLSID'22), Hyderabad, India, 2022.

C5. A Hardware Implementation of the kCAS Synchronization Primitive by Srishty Patel, Rajshekar Kalayappan, Ishani Mahajan, Smruti R. Sarangi, Design, Automation and Test in Europe (DATE'17), Lausanne, Switzerland, 2017.

C6. SecCheck : A Trustworthy System with Untrusted Components by Rajshekar Kalayappan, Smruti R. Sarangi, IEEE Computer Society Annual Symposium on VLSI (ISVLSI'16), Pittsburgh, USA, 2016.

C7. SecX: A Framework for Collecting Runtime Statistics for SoCs with Multiple Accelerators by Rajshekar Kalayappan, Smruti R. Sarangi, IEEE Computer Society Annual Symposium on VLSI (ISVLSI'15), Montpellier, France, 2015.

C8. Tejas: A java based versatile micro-architectural simulator by Smruti R. Sarangi, Rajshekar Kalayappan, Prathmesh Kallurkar, Seep Goel, Eldhose Peter, IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS'15), Salvador, Brazil, 2015.

Patents

P1. Providing Accountability in Heterogeneous SoCs Using Dual Metering, by Smruti R. Sarangi, Rajshekar Kalayappan. Indian patent granted: 523610.

P2. Parallelization of a Trace-Driven Architectural Simulator, by Smruti R. Sarangi, Rajshekar Kalayappan, Avantika Chhabra (under process)

Sponsored Projects

P1. Criticality-aware Hybrid Cache Hierarchy, PI: Rajshekar K, SERB Core Research Grant. 2021 – 2023. Completed.

Professional Service and Activities

✠ Reviewer

- Journals: TCAD, CSUR, JSA, ESL
- Conferences: MICRO, ASPLOS, IPDPS, HiPC, VLSID, CASES
- Funding proposals submitted to Science and Engineering Research Board, Government of India, and the National Supercomputing Mission, Government of India

✠ Committee Member

- Member of the Board of Studies of the Department of Computer Science and Engineering at SDM College of Engineering, Dharwad, India
- Session chair at Embedded Systems Week (ESWEEK) 2022
- Member of the Program Committee of the International Conference on High Performance Computing, Data, and Analytics (HiPC) 2019
- Member of the Program Committee of the IC3 conference 2018

Date: 15^{th} February, 2024
Place: Dharwad, India (Rajshekar K)