SEMESTER III – Electrical Engineering

Course Code	Course Name	L	T	P	Total Credits	Course Instructor
EE 201	Data Analysis	3	0	0	6	Prof. Sudhanshu Shukla (SS)
EE 203	Electronic Devices	3	0	0	6	Prof. Ruma Ghosh (RG)
EE 205	Network Theory	2	1	0	6	Prof. S. R. M. Prasanna (SRMP)
EE 207	Signals and Systems	2	1	0	6	Prof. Naveen Kadayanti (NK)
HS 201	Economics	3	0	0	6	Prof. Haripriya Gundimeda ((HG) / Prof. Pushpa Trivedi (PT)
MA 201	Complex Analysis	3	1	0	4	Prof. Amlan Barua (AB)
MA 203	Differential Equations-II	3	1	0	4	Prof. Amlan Barua (AB)
Total Credits					**38**	

Fifth (V) Semester – EE (2016 Batch)

Course Code	Course Name	Course Structure				Course instructor
		L	T	P	Total Credits	
CS 301	Computer Architecture	3	0	0	6	Prof. Rajshekar K. (RK)
EE 303	Control Systems	3	0	0	6	Prof. Ameer K. M. (AKM)
EE 305	Digital Signal Processing	3	0	0	6	Prof. S. R. M. Prasanna (SRMP)
EE 307	Probability and Random Process	3	0	0	6	Prof. Bharath B. N. (BBN)
	HSS elective - I	3	0	0	6	
CS 311	Computer Architecture lab	0	0	3	3	Prof. Rajshekar K. (RK)
EE 311	Electrical Machines and Power electronics lab	0	0	3	3	Prof. Ameer K. M. (AKM) / Prof. Bharath B. N. (BBN)
Total Credits					**36**	

HSS Elective - I						
HS 301	Philosophy	3	0	0	6	Prof. C. D. Sebastian (CDS)
HS 303	Introduction to Literature	3	0	0	6	Prof. Ridhima Tewari (RT)

INDIAN INSTITUTE OF TECHNOLOGY DHARWAD

EE UG Course
Time Table for Autumn Semester 2018-19

COURSE NO.	COURSE NAME	INSTRUCTOR	ROOM NO.	Remarks
SLOT 1	**1A (M 8.30-9.25), 1B (Tu 9.30-10.25), 1C (Th 11.00-11.55)**			
EE 203	Electronic Devices	RG	115	
SLOT 1	**1A (M 8.30-9.25), 1B (Tu 9.30-10.25)**			
CS 301	Computer Architecture	RK	210	
SLOT 2	**2A (M 9.30-10.25), 2B (Tu 11.00-11.55), 2C (Th 12.00-12.55)**			
MA 201/ MA 203	Complex Analysis/ DE II	AB	115	
EE 305	Digital Signal Processing	SRMP	211	
SLOT 3	**3A (M 11.00-11.55), 3B (Tu 12.00-12.55), 3C (Th 8.30-9.25)**			
EE 207	Signals and Systems	NK	115	
EE 307	Probability and Random Processes	BBN	211	
SLOT 4	**4A (M 12.00-12.55), 4B (Tu 8.30-9.25), 4C (Th 9.30-10.25)**			
EE 201	Data Analysis	SS	23	
SLOT 4	**4A (M 12.00-12.55), 4C (Th 9.30-10.25)**			
EE 303	Control Systems	AKM	211	
	4B (Tu 8.30-9.25)			
HSS Elective	Philosophy	CDS	210	
SLOT 5A	**5A (W 9.30-10.55)**			
	Introduction to Literature	RT	211	
	5A (W 8.30-9.25)			
HSS Elective	Philosophy	CDS	210	
SLOT 5B	**5B (F 9.00-10.25)**			
HS 201	Economics	HG/PT	23	
SLOT 6	**6A (W 11.05-12.30), 6B (F 11.05-12.30)**			
MA 201/ MA 203	6B - Complex Analysis/ DE II	AB	115	
EE 303	6B - Control Systems	AKM	211	
SLOT 6	**6C (W 8.30-9.25)**			
CS 301	Computer Architecture	RK	210	
SLOT 7	**7A (W 17.05-18.00)**			
SLOT 8	**8A (M 14.00-15.25), 8B (TH 14.00-15.25)**			

SLOT 9	**9A (M 15.30-16.55), 9B (TH 15.30-16.55)**			
SLOT 10	**10A (TU 14.00-14.55), 10B (F 14.00-15.25)**			
HSS Elective	10A – Philosophy	CDS	210	
	10B - Introduction to Literature	RT	211	
SLOT 11	**11A (TU 15.30-16.55), 11B (F 15.30-16.55)**			
HS 201	11B - Economics	HG	23	
SLOT 12	**12A (M 17.30-18.55), 12B (TH 17.30-18.55)**			
HS 201	12B - Economics	HG	23	
			211	
SLOT 13	**13A (M 19.00-20.25), 13B (TH 19:00-20.25)**			
			117	
			211	
SLOT 14	**14A (TU 17.30-18.55), 14B (F 17.30-18.55)**			
			117	
			211	
SLOT 15	**15A (TU 19:00-20:25), 15B (F 19:00-20:25)**			
			117	
			211	
SLOT XC	**(W 17:00-18:30)**			
			117	
			211	
SLOT 16	**16A (SAT 8.30-9.55) 16B (SAT 10.30-11.55)** **16C (SAT 13.30 – 14.55)**			
HS 201	16A - Economics	HG	23	
EE 205	16B - Network Theory		115	
EE 205	16C - Network Theory		115	

L1 (M 14.00- 16.55)	**L2 (Tu 14.00-16.55)**	**L3 (Th 14.00-16.55)**	**L4 (F 14.00-16.55)**	
L5 (W 9.30-12.30)	**L6 (F 9.30-12.30)**	**LX (W 14.00-16.55)**	**X3 (W 16.00-17.00)**	
LM (M 9.30-12.30)	**LT (Tu 9.30-12.30)**	**LH (Th 9.30-12.30)**		
Lab Timetable	**Course Name**	**Instructor**	**Room No.**	**Slot**
CS 311	Computer Architectures Lab	RK		L4
EE 311	Electrical Machines and Power Electronics Lab			L3