INDIAN INSTITUTE OF TECHNOLOGY DHARWAD

Department of Electrical Engineering
Ph.D. Admissions Brochure
Spring-2018

A. SCHEDULE OF PH.D. ADMISSION

S. No.	Particulars	Dates
1	Advertisement (in all leading Newspapers and on website)	
2	Availability of online application forms	
3	Last date for submission of completed application forms	~~31st October, 2018~~ 13th November, 2018
4	List of shortlisted candidates for the Selection Process[1]	~~06th November, 2018~~ 15th November, 2018
5	Dates for the Selection Process	10th and 11th of December, 2018
6	Declaration of Result[1]	15th December, 2018
8	Last date for Fee Payment (at IITDh)	21st December, 2018
7	Date of Joining	28th December, 2018
8	Last date of withdrawal	31st December, 2018

B. ELIGIBILITY FOR ADMISSION

Qualifying Degree: M.Tech./M.E. or equivalent degree, with good academic records, in the relevant specializations (to the candidate's preferred area of research) of either, Electrical Engineering, Electronics and (Tele)Communication Engineering, Computer Science Engineering, and Instrumentation and Control Engineering or equivalent specializations.

B.1. Minimum score in the qualifying degree

For General/OBC category candidates and/or for candidates where no concession in academic performance is called for, the eligibility criteria in the qualifying degree

[1] Will be announced on the institute webpage.

(M.Tech./M.E. or equivalent) AND the Bachelor's Degree (B. E./B. Tech./M. Sc or equivalent) is **First Class** as specified by the University. If the University doesn't specify the division/class, then either:

1. a minimum of 60% marks (without round off) in aggregate.
2. a minimum Cumulative Grade Point Average (CGPA) or Cumulative Performance Index (CPI) of 6.0 on the scale of 0-10; with corresponding proportional requirements when the scales are other than on 0-10, (for example, 4.8 on a scale of 0-8).

For SC/ST category candidates and differently abled candidates (PwD), a relaxation of 5% (or CPI/CGPA of 0.5 on the scale of 0-10) in the qualifying degree is applicable.

C. APPLICATION CATEGORIES AND FINANCIAL SUPPORT

The Department of Electrical Engineering admits candidates for full time Ph. D. Programme, under Teaching Assistantship (TA), Financial Assistantship (JRF from UGC/CSIR NET, INSPIRE Fellowship etc) and External (EX) schemes only.

C.1. Teaching Assistantship (TA)

The students admitted as TAs are Funded by MHRD. The TAs are expected to assist in the academic/administrative work for smooth functioning of the Institute. Students under this category are entitled to financial support as per MHRD norms in force.

At present, the assistantship is payable for a maximum duration of 5 years or up to the defence of the thesis, whichever is earlier, at the monthly rate of ₹ 25,000 for the first 2 years and enhanced rate of ₹ 28,000/- for the remaining period, subject to satisfactory performance in academics and assigned TA duties.

To get Teaching Assistantship, the concerned students must assist in teaching, research and/or administrative work as assigned by the respective Academic Unit to the extent of 8 hours of work per week. The continuation of the assistantship will be subject to satisfactory performance of the duties assigned by the Departments as well as satisfactory academic performance.

As per MHRD directives, the employees of any organizations with or without pay are not eligible for admission under TA category. Candidates selected in this category have to resign from the current job and submit a relieving letter from their employer before joining the programme. Students getting assistantships from the Institute may join projects sponsored by external agencies and obtain corresponding fellowships in lieu of TA ship.

C.2. Financial Assistantship (FA)

The students admitted under FA category are financially supported under various Govt. / Semi Govt. schemes like JRF of CSIR/UGC, DST INSPIRE etc. For admission under this category, the applicant must have qualified for funding though one of such schemes. The admission procedure and other requirements are same as applicable to TA.

C.3. External (EX)

The candidates employed in recognized R&D organizations and desirous of pursuing Ph.D. programme while in employment may apply for admission as external candidates. After fulfilling the coursework requirement at the Institute, these candidates will be allowed to register for Ph.D. with a Supervisor (internal) from the Institute and a Co-supervisor (external) from their parent organization where they will be doing the research work. The admissions are based on the following norms: i. The competence of these candidates will be assessed along with the regular candidates.

ii. The candidate should submit at the time of application, a Sponsorship Certificate (Appendix A.1) from the organization in which he/she is employed giving an undertaking that the candidate would be released from the normal duties to fulfill the coursework requirement (and qualifier examination, if applicable). The certificate should also provide details of facilities relevant to the research programme and available to the candidate.

iii. The candidate is required to be at the Institute as a full-time student for the coursework (and qualifier examination, if applicable) of his/her Ph.D. Programme. The coursework requirement is likely to be a period of 1-2 semesters. Depending on the student's background and the programme requirements, an additional semester may be needed to complete the coursework/qualifier examination.

iv. To promote interaction between the internal supervisor and external co-supervisor, meeting between them should be arranged at least once in a year in the Institute or in the sponsoring organization.

v. The Ph.D. registration of an external candidate would be reviewed at the end of each year from the date of registration in terms of his progress in courses / seminars / approved research programme by a Research Progress Committee (RPC) nominated by the concerned Department Postgraduate Committee (DPGC).

vi. The option of external registration is for applicants who are working in well-equipped scientific institutions, laboratories, R&D establishments and industrial organizations engaged in research based activities. Persons working in colleges/universities are **NOT** eligible under this category. vii. At the time of joining the programme, the students will have to produce a “Relieving certificate” from his / her employer that he / she has been fully relieved from normal duties during the semester(s) to complete the course work and other academic work at IIT Dharwad

Based on the information provided by the applicants a short-list of candidates called for the selection process will be declared on the Institute website on the date specified in the schedule. Only the short-listed candidates are permitted to participate in the selection process.

D. GUIDELINES FOR SHORTLISTED APPLICANTS

The following are the important guidelines of the institute pertaining to the selection process

1. **Reporting Time: 10th December, 2018 at 9:00 AM.**
2. **Screening test will begin on 10th December, 2018 at 10:30AM.**
3. Based on the performance in the screening test, some of the candidates will be shortlisted for the first interview.

4. Based on the performance in the first interview, some of the candidates will be shortlisted for the second interview.

5. Interviews will be held immediately after the short-list is declared. **Please note that the interviews may extend to the next day i.e. 11th December, 2018.**
6. **No accommodation can be provided** in the campus during the written/interview.
7. Applicants should bring:
    a. Photo ID card
    b. Printed copy of the application
    c. Thesis/dissertation/report of M.Tech. or equivalent degree
    d. Copy of certificates and mark-sheets
    e. Two passport size photographs
    f. Non-programmable scientific calculator

D.1. DO NOT's

a. Mobile phones are not allowed in the examination hall or in the interview room
b. Department's decision is the final decision regarding any matter pertaining to this selection process.
c. Institute doesn't take any responsibility of your luggage/items that you leave before entering the examination hall.

E. MODALITY OF THE SELECTION PROCESS

Only the short-listed applicants are permitted to participate in the selection process.

The selection process consists of a screening test followed by interview(s). The screening test will either be online or written.

Based on the performance in the screening test, some of the candidates will be short-listed for the interviews. The details of the screening test and interview are given in the following sections.

E.1. Details about the screening test

1. Screening test is a 60-minute test for all the short-listed applicants.

2. Based on the preferred area of the research (first choice), candidates will write test in any **one** of the following streams.

    a) Communication and Signal Processing

    b) Control and Robotics

    c) Electronic Devices and Mixed signal ASIC design

    d) Power and Energy Systems

    Changes in the subject or preferences for areas of research are NOT permitted after submission of the application form.

3. The syllabus for the screening test is given in Section G of this document. Apart from the prescribed syllabus, the test may contain questions based on general aptitude and reasoning.
4. After the screening test, candidates are instructed to wait till the short-list for the interview round is displayed on the notice board
5. Interviews will begin immediately after the display of the short-list. It is the responsibility of the candidate to be present at the venue, when (s)he is called for the interview. **No personal intimation will be given after the screening test.**

E.2. Details about the interviews

1. Faculty from all fields and from other departments may be present in the interview panel
2. The final list of selected applicants will be announced on the specified date.

F. RESEARCH TOPICS

The research topics are broadly classified in three areas as described below. The applicant MUST indicate the choice of the research topics in the order of preference.

1. **Signal Processing:** Including but not limited to, Emotional analytics, Speech Processing, Handwriting and Document Processing, Speech Interfaces for Robotics, Signal Processing/Machine Learning methods for Communications

2. **Communication Technologies:** Including but not limited to, physical and medium access control (MAC) layer technologies in Next Generation Wireless Systems (5G and beyond), Internet of Things (IoT), novel multiple access methods like nonorthogonal multiple access (NOMA), massive multi-input multi-output (MIMO) systems, millimetre wave (mmWave) communications, etc.

3. **Control and Robotics:** Including but not limited to Control of Robots through Speech Signals, Autonomous Vehicles, Control for Differential Games, Control of Structures etc.

4. **Electronic Devices:** Including but not limited to Gas sensors, Nano-electronics etc.

5. **Mixed signal ASIC Design:** This area is related to practical mixed signal integrated circuits. Topic could be one of high speed interconnects, circuits and systems for instrumentation, design for testability of mixed signal circuits etc. Work will include the design of integrated circuits, from concept formulation to verification of ideas in hardware with a prototype chip.

6. **Power and Energy Systems:** Power system dynamics and control, synchrophasor applications to power systems protection, monitoring and control, control applications to power system and microgrid.

G. SYLLABUS FOR THE WRITTEN TEST

A. Engineering Mathematics: Common for all the streams

1. **Linear Algebra:** Matrix Algebra, Systems of linear equations, Eigenvalues, Eigenvectors.
2. **Real Analysis/Calculus:** Concepts from sequences, limits, series, functions, integration and differentiation.
3. **Transform Theory:** Fourier Transform, Laplace Transform, z-Transform.

B. Communication and Signal Processing

1. **Signals and Systems:**
   a) **Continuous-time signals:** Fourier series and Fourier transform representations, sampling theorem and applications;
   b) **Discrete-time signals:** discrete-time Fourier transform (DTFT), DFT, FFT, Z-transform, interpolation of discrete-time signals;
   c) **LTI systems:** definition and properties, causality, stability, impulse response, convolution, poles and zeros, parallel and cascade structure, frequency response, group delay, phase delay, digital filter design techniques.
   d) **Random processes:** basics of probability, random variables, CDF, PDF, random processes, mathematical expectation, conditional probability and conditional expectation, correlation, covariance and moment generating function.
2. **Communication:**
   a) **Random processes:** basics of probability, random variables, CDF, PDF, random processes, mathematical expectation, conditional probability and conditional expectation, correlation, covariance and moment generating function.
   b) **Information theory:** entropy, mutual information and channel capacity theorem;
   c) **Digital communications:** Digital modulation schemes, MAP and ML decoding, notions of bandwidth, SNR and BER for digital modulation; Fundamentals of error correction, Basics of TDMA, FDMA and CDMA, knowledge of OSI layers.

C. Control and Robotics:

Mathematical modeling and representation of systems, Basic control system components, Feedback principle, Transfer function, Block diagram representation, Signal flow graph,
Transient and steady -state analysis of LTI systems, Frequency response, Stability analysis, Routh-Hurwitz and Nyquist stability criteria, Bode plots, Nyquist plots and root-loci, P, PI and PID controllers, Lag, lead and lag-lead compensation, State-space representation, Statetransition matrix, and solution of state equation of LTI systems, Controllability and Observability, Design of state-feedback controllers, Luenberger Observer, Time-delay systems, mechanical, hydraulic and pneumatic system components, servo and stepper motors, on-off control, principle of optimality, dynamic programming, Pontryagin's Maximum Principle.

D. Electronic Devices and Mixed signal ASIC Design:

1. **Electronic Devices:** Energy bands in intrinsic and extrinsic silicon; Carrier transport: diffusion current, drift current, mobility and resistivity; Generation and recombination of carriers; Poisson and continuity equations; P-N junction, Zener diode, BJT, MOS capacitor, MOSFET, LED,

photo diode and solar cell; Integrated circuit fabrication process: oxidation, diffusion, ion implantation, photolithography and twin-tub CMOS process.

2. **Analog Circuits:** Small signal equivalent circuits of diodes, BJTs and MOSFETs; Simple diode circuits: clipping, clamping and rectifiers; Single-stage BJT and MOSFET amplifiers: biasing, bias stability, mid-frequency small signal analysis and frequency response, multistage, differential, feedback, power and operational; Simple op-amp circuits; Active filters; Sinusoidal oscillators: criterion for oscillation, single-transistor and op-amp configurations; Function generators, wave-shaping circuits and 555 timers; Voltage reference circuits; Power supplies: ripple removal and regulation.
3. **Digital Systems:** Number systems; Combinatorial circuits; Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits, code converters, multiplexers, decoders and PLAs;

   Sequential circuits: latches and flip-flops, counters, shift-registers and finite state machines; Data converters: sample and hold circuits, ADCs and DACs.

E. Power Systems:

1. **UG Power System:** Power flow, power system protection, faults, stability.
2. **Power system dynamics:** synchronous machine modelling, transient stability, small signal stability, power system stabilizer, load frequency control, subsynchronous resonance.
3. **Renewable Energy**: modelling of PV and DFIG.
4. **Linear Control System**: Mathematical modeling and representation of systems, Basic control system components, Feedback principle, Transfer function, Block diagram representation, Signal flow graph, Transient and steady -state analysis of LTI systems, Frequency response, Stability analysis, Routh-Hurwitz and Nyquist stability criteria, Bode plots, Nyquist plots and root-loci, P, PI and PID controllers, Lag, lead and lag-lead compensation, State-space representation, State-transition matrix, and solution of state equation of LTI systems, Controllability and Observability, Design of state-feedback controllers.

Appendix A.1

Format for Sponsorship Certificate for Ph.D. External Registration (EX)

(To be typed on letterhead of the Sponsoring Organization)

Name of the sponsoring organization: _____

Address: _____
_____
_____

Present Designation of the applicant: _____

Present status of the applicant: _____
(Permanent/Quasi Permanent/Temporary)

Division where research work is proposed to be done:

_____

Name of supervisor from the sponsoring organization: _____

(Bio-data of supervisor to be enclosed giving details of designation, qualification, research experience etc. *Note: The supervisor from the sponsoring organization should be a Ph.D. holder)*

Details of facilities relevant to the research problem which will be made available to the candidate by the organization.

Declaration by proposed Co-supervisor (external)

If Shri / Kum. / Smt._____ is registered for the doctorate degree, I agree to act as his/ her research Co-supervisor along with the research Supervisor from IIT Dharwad.

Signature of proposed Co-supervisor (external)

Contd.

If Shri./ Kum./ Smt. _____ is admitted to the Ph.D. programme, we shall allow him/ her to undergo the programme of studies at IIT Dharwad.

Further, if Shri./ Kum./ Smt. _____ is admitted to the Ph.D. programme, we shall fully relieve him/her from normal duties to complete the course work requirement (and qualifier examination, if applicable) at IIT Dharwad.

During the period of Doctoral programme, the candidate will be permitted to carry out his / her research work at our laboratories / organization and will be given the required facilities.

We also give our consent to _____ of our organization to be the Co-supervisor (external) of the Ph.D. thesis, along with a faculty member of IIT Dharwad as the Supervisor.

Signature and Seal of the Sponsoring Authority

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